AMENDMENTS TO THE CLAIMS

Claims 1-67 cancelled.

68. (Original) A method for manufacturing a semiconductor device comprising the steps of:

forming a first insulating film on a surface of an active region of a semiconductor substrate;

forming a first conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a first predetermined concentration into said first conductive film by ion injection;

forming a second insulating film on said first conductive film above at least said active region except for an element isolation region of said semiconductor substrate;

forming a second conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a second predetermined concentration higher than said first predetermined concentration into said second conductive film by thermal diffusion; and

patterning a lamination of said first conductive film and said second conductive film to a predetermined shape.

69. (Original) A method as claimed in claim 68, wherein said second insulating film includes a nitride film.

70. (Original) A method as claimed in claim 68, wherein said second insulating film is a multilayer insulating film containing an oxide film and a nitride film.

71. (Original) A method as claimed in claim 68, wherein each of said first conductive film and said second conductive film is made of a material containing silicon.

72. (Original) A method as claimed in claim 68, wherein said first impurity concentration is $1x10^{18}$ to $1x10^{19}$ atoms/cm^3 and said second impurity concentration is $1x10^{20}$ to $1x10^{21}$ atoms/cm^3.

73. (Original) A method as claimed in claim 68, wherein the lamination of said first conductive film and said second conductive film is patterned in said patterning step in a shape of a composite gate structure of a transistor.

74. (Original) A method as claimed in claim 68, wherein the lamination of said first conductive film and said second conductive film is patterned in said patterning step in a shape of a single gate structure of a transistor.

75. (Original) A method for manufacturing a semiconductor device comprising the steps of:

forming a first insulating film on a surface of an active region of a semiconductor substrate;

forming a first conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a first predetermined concentration into said first conductive film by ion injection;

forming a second insulating film on said first conductive film;

forming a second conductive film over an entire surface of said semiconductor substrate;

introducing an impurity at a second predetermined concentration higher than said first predetermined concentration into said second conductive film by thermal diffusion; and

patterning a lamination of said first conductive film and said second conductive film to a predetermined shape.

76. (Original) A method as claimed in claim 75, wherein said patterning step includes a substep of patterning a lamination of said second conductive film, said second insulating film, and said first conductive film to a first predetermined shape in said active region, and patterning a lamination of said second conductive film and said first conductive film into a second predetermined shape in an element isolation region of said semiconductor substrate.

77. (Original) A method as claimed in claim 75, wherein said second insulating film includes a nitride film.

78. (Original) A method as claimed in claim 75, wherein said second insulating film is a multilayer insulating film containing an oxide film and a nitride film.

79. (Original) A method as claimed in claim 75, wherein each of said first conductive film and said second conductive film is made of a material containing silicon.

80. (Original) A method as claimed in claim 75, wherein said first impurity concentration is $1x10^{18}$ to $1x10^{19}$ atoms/cm^3, and said second impurity concentration is $1x10^{20}$ to $1x10^{21}$ atoms/cm^3.

81. (Original) A method as claimed in claim 75, wherein in said patterning step, the lamination of said first conductive film and said second conductive film is patterned in. a shape of a composite gate structure of a transistor.

82. (Original) A method as claimed in claim 75, wherein the lamination of said first conductive film and said second conductive film is patterned in said patterning step in a shape of a single gate structure of a transistor.

Claims 83-95 cancelled.